REMARKS

In the Office Action of March 19, 2004, the Examiner requested confirmation of the provisional election of March 11, 2004 of Group I, which includes claims 1-8 and 14-20; rejected claims 1-8, 14-18, and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,657,259 to Fried et al. ("Fried") in view of U.S. Patent No. 6,589,836 to Wang et al. ("Wang"); and rejected claim 19 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fried in view of Wang and further in view of published U.S. Patent Application No. US 2001/0045589 to Takeda et al. ("Takeda").

By way of this amendment, a typographical error in the specification has been corrected and claims 1 and 14 have been amended to improve form. Claim 8-13 and 20 were canceled without prejudice or disclaimer and claims 21-23 were added. Claims 1-7, 14-19, and 21-23 are now pending.

IDS

At the outset, Applicants note that the Examiner considered the Information Disclosure Statement (IDS), filed on July 8, 2003. Applicants, however, note that a second IDS was filed on October 23, 2003 and a copy of the initialed PTO-1449 was not returned with this Office Action. Applicants respectfully request that this IDS be considered by the Examiner and an initialed copy of the PTO-1449 be returned to Applicants with the next communication. A copy of form PTO-1449 previously filed on October 23, 2003 is included herewith for the Examiner's convenience.

CONFIRMATION OF PROVISIONAL ELECTION

Applicants confirm the election of Group I, which now includes claims 1-7 and 14-19. Applicants submit that new claims 21-23 are also included in Group I.

REJECTION OF CLAIMS 1-8, 14-18 AND 20

Claims 1-8, 14-18, and 20 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fried in view of Wang. Applicants respectfully traverse the rejection. The rejection is moot with respect to claims 8 and 20, which were canceled without prejudice or disclaimer.

Amended independent claim 1 recites a semiconductor device. The semiconductor device includes, among other things, a first device formed on an insulating layer, including a first fin formed on the insulating layer and a first silicided gate formed over a portion of the first fin and including a first thickness of silicide material. The semiconductor device also includes a second device formed on the insulating layer, including a second fin formed on the insulating layer and a second silicided gate formed over a portion of the second fin and including a second thickness of silicate material different from the first thickness. Claim 1, as amended, further recites that a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

Fried relates to multiple-plane FinFET complementary metal oxide semiconductor (CMOS) technologies (see Fried at column 1, lines 6-8).

Wang relates to a method for forming thin salicide on elements of a P channel metal oxide semiconductor (PMOS) device, while simultaneously forming thicker salicide on elements of an N channel metal oxide semiconductor (NMOS) device (see Wang at column 1, lines 9-14).

Applicants submit that, neither Fried nor Wang disclose or suggest, either separately, or in combination, the above-mentioned features of amended independent claim 1. For example, Fried and Wang do not disclose or suggest that a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

On page 5 of the Office Action, the Examiner argued that Fried in view of Wang discloses a semiconductor device in which a threshold voltage of a first device is lower than a threshold voltage of a second device because varying the thickness of silicide layers inherently varies threshold voltages. Applicants submit that, even if the Examiner's argument is true (a point which Applicants do not concede) Fried and Wang do not disclose or suggest, either separately or in combination, a semiconductor device in which a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device, as recited in claim 1. Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-7 depend from claim 1 and are patentable over Fried in view of Wang for at least the reasons discussed above with respect to claim 1. Therefore, Applicants respectfully request that the rejection of claim 2-7 be withdrawn.

Claim 14 recites a semiconductor device that includes a substrate, an insulating layer, a first device and a second device. The insulating layer is formed on the substrate. The first device is formed on the insulating layer. The first device includes a first fin formed on the insulating layer, a first dielectric layer formed on the first fin, and a partially silicided gate formed over a portion of the first fin and the first dielectric layer. The second device is formed on the insulating layer. The second device includes a second fin formed on the insulating layer, a second dielectric layer formed on the second fin, and a fully silicided gate formed over a portion of the second fin and the second dielectric layer. A threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

As stated above, neither Fried nor Wang discloses or suggests, either separately or in combination, a semiconductor device in which a threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of a first device, as recited in claim 14. Applicants also note that Wang discloses that both devices include partially silicided gate structures (see Figs. 6 and 7). Claim 14, in contrast, recites that the first device includes a partially silicided gate and the second device includes a fully silicided gate. Therefore, Applicants submit that claim 14 is patentable over Fried in view of Wang and respectfully requests that the rejection of claim 14 be withdrawn.

Claims 15-18 depend from claim14 and are patentable for at least the reasons discussed above with respect to claim 14. Therefore, Applicants submit that claims15-18

are patentable over Fried in view of Wang and respectfully request that the rejection of claims 15-18 be withdrawn.

REJECTION OF CLAIM 19

Claim 19 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fried in view of Wang and further in view of Takeda. Applicants respectfully traverse the rejection.

Claim 19 depends from amended claim 14. Claim 14 is patentable over Fried and Wang for at least the reasons discussed above with respect to claim 14.

Takeda relates to a semiconductor device having multiple basic units, each containing a memory cell and a logic cell on the same semiconductor substrate (see Takeda at column 1, paragraph 3). However, Takeda fails to cure the deficiencies of Fried and Wang and does not disclose a semiconductor device in which a threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of a first device, as recited in claim 14. Therefore, Applicants respectfully request that the rejection of dependent claim 19 be withdrawn.

NEW CLAIMS 21-23

New claims 21-23 depend either from claim 1 or claim 14 and are patentable over the cited references at least for the reasons discussed above with respect to claims 1 and 14. In addition, the claims recite features not disclosed or suggested by the cited art.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: Richard C. Irving

Richard C. Irving
Registration No. 38,499

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
Telephone: (571) 432-0800
Facsimile: (571) 432-0808